IN THE SPECIFICATION:

Please amend the specification as shown below.

On page 1, lines 6-29, please revise as follows:

The following related patent applications~~, all filed on July 30, 1999,~~ are hereby incorporated by reference in their entirety for all purposes:

U.S. Patent Application Serial No. 09/364,512, entitled "Processor with Improved Accuracy for Multiply-Add Operations," by Ying-wai Ho, John Kelley, and James Jiang, filed on July 30, 1999;

U.S. Patent Application Serial No. 09/364,514, entitled "Floating-Point Processor with Improved Intermediate Result Handling," by John Kelley and Ying-wai Ho, filed on July 30, 1999;

U.S. Patent Application Serial No. 09/363,638, entitled "Method and Apparatus for Predicting Floating-Point Exceptions," by James Jiang, Ying-wai Ho, and John Kelley, filed on July 30, 1999;

U.S. Patent Application Serial No. 09/363,637 ~~09/334,927~~, entitled "System and Method for Improving the Accuracy of Reciprocal and Reciprocal Square Root Operations Performed by a Floating-Point Unit," by Ying-wai Ho, Michael Schulte, and John Kelley, filed on July 30, 1999;

U.S. Patent Application Serial No. 10/055,346, entitled "System and Method for Improving the Accuracy of Reciprocal Square Root Operations Performed by a Floating-Point Unit," by Ying-wai Ho, Michael Schulte, and John Kelley, filed on January 25, 2002, which is a divisional of 09/363,637;

U.S. Patent Application Serial No. 09/364,786, entitled "Processor Having a Compare Extension of an Instruction Set Architecture," by Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell, filed on July 30, 1999;

U.S. Patent Application Serial No. 09/364,789, entitled "Processor Having a Conditional Branch Extension of an Instruction Set Architecture," by Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell, filed on July 30, 1999; and

a1

U.S. Patent Application Serial No. 09/364,787, entitled "Processor Having an Arithmetic Extension of an Instruction Set Architecture," by Radhika Thekkath, Michael Uhler, Ying-wai Ho, and Chandlee Harrell, filed on July 30, 1999.

On page 19, lines 24-32, please revise as follows:

a2

Many of the steps shown in Fig. 6 are normally performed in floating-point processors, such as those described in the aforementioned Patent Application Serial Nos. 09/363,638, 09/364,514, 09/364,512, 09/363,637 ~~09/334,927~~, 09/364,786, 09/364,789, and 09/364,787. To implement the flush-to-nearest mode of the invention, step 612 is modified to include the check to determine whether the exponent is equal to E_{min} -1 and steps 620 and 622 are added. It can be noted that in these steps, only the preliminary exponent, Exp, is checked to determine whether it is equal to E_{min} - 1. The additional steps can be easily achieved with small implementation cost and can be executed with small or no additional processing delay.